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FROM: Winston Hsu, PATENT AGENT, REG. NO. : 41,526

SERIAL NO.: 10/708,638

ATTORNEY DOCKET NO.: VIAP0101USA

SUBJECT: INFORMATION DISCLOSURE STATEMENT

TOTAL PAGES: 16 PAGES (INCLUDING COVER PAGE)

Winston Hsu 2004/09/15

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PTO/SB/97 (08-03)

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APPLICATION NUMBER: 10/708,638

PAPERS INCLUDED:

(1) Transmittal Form	1 PAGE
(2) Fee Transmittal	1 PAGE
(3) Information Disclosure Statement	12 PAGES

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TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>	Application Number	10/708,638	
	Filing Date	03/17/2004	
	First Named Inventor	Chi-Yang Lin	
	Art Unit	2673	
	Examiner Name		
Total Number of Pages in This Submission	14	Attorney Docket Number	VIAP0101USA

ENCLOSURES (Check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance communication to Technology Center (TC)
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Amendment/Reply	<input type="checkbox"/> Petition	<input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
<input type="checkbox"/> After Final	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Proprietary Information
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<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD, Number of CD(s) _____	
<input type="checkbox"/> Response to Missing Parts/Incomplete Application	Remarks	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Winston Hsu, Reg. No.: 41,526
Signature	<i>Winston Hsu</i>
Date	9/15/2004

CERTIFICATE OF TRANSMISSION/MAILING			
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FEE TRANSMITTAL
for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT**

(\$ 0.00)

Complete if Known

Application Number 10/708,638

Filing Date 03/17/2004

First Named Inventor Chi-Yang Lin

Examiner Name

Art Unit 2673

Attorney Docket No. VIAP0101USA

METHOD OF PAYMENT (check all that apply)☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☒ Deposit Account:Deposit
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☒ Charge fee(s) indicated below ☒ Credit any overpayments☒ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 770	2001 385	Utility filing fee	
1002 340	2002 170	Design filing fee	
1003 530	2003 265	Plant filing fee	
1004 770	2004 385	Reissue filing fee	
1005 160	2005 80	Provisional filing fee	

SUBTOTAL (1) (\$ 0.00)**2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE**

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent Claims	-20** =	X	
Multiple Dependent	-3** =	X	

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
1202 18	2202 9	Claims in excess of 20
1201 88	2201 43	Independent claims in excess of 3
1203 290	2203 145	Multiple dependent claim, if not paid
1204 88	2204 43	** Reissue independent claims over original patent
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$ 0.00)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	1053 130	Non-English specification	
1812 2,520	1812 2,520	For filing a request for ex parte reexamination	
1804 920*	1804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	1805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 420	2252 210	Extension for reply within second month	
1253 950	2253 475	Extension for reply within third month	
1254 1,480	2254 740	Extension for reply within fourth month	
1255 2,010	2255 1,005	Extension for reply within fifth month	
1401 330	2401 165	Notice of Appeal	
1402 330	2402 165	Filing a brief in support of an appeal	
1403 290	2403 145	Request for oral hearing	
1451 1,510	1451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,330	2453 665	Petition to revive - unintentional	
1501 1,330	2501 665	Utility issue fee (or reissue)	
1502 480	2502 240	Design issue fee	
1503 640	2503 320	Plant issue fee	
1460 130	1460 130	Petitions to the Commissioner	
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)	
1806 180	1806 180	Submission of Information Disclosure Stmt	
8021 40	8021 40	Recording each patent assignment per property (times number of properties)	
1809 770	2809 385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 770	2810 385	For each additional invention to be examined (37 CFR 1.129(b))	
1801 770	2801 385	Request for Continued Examination (RCE)	
1802 900	1802 900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basis Filing Fee Paid

SUBTOTAL (3) (\$ 0.00)**SUBMITTED BY**

Name (Print/Type) Winston Hsu

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(Attorney/Agent)

(Complete if applicable)

Telephone 886289237350

Signature

Date

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PATENT
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant(s): Chi-Yang Lin, Peter Chen
5 Filing Date: 03/17/2004
Art Unit: 2673
Serial No.: 10/708,638
Docket No.: VIAP0101USA

SEP 15 2004

10 Title: DISPLAY CONTROLLER AND RELATED METHOD FOR CALIBRATING
DISPLAY DRIVING VOLTAGES ACCORDING TO INPUT RESISTANCE
OF A MONITOR

15 To: Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Subject: Information disclosure statement under
37C.F.R. \$1.56 and 37C.F.R. \$1.97(b).

20

Dear Sir/Madam:

25 This is an Information Disclosure Statement in accordance
with the duty to disclose information material to
patentability under 37 C.F.R. \$1.56. Applicants wish to make
of record the document listed on the accompanying form
PTO/SB/08. It is respectfully requested that the Examiner
initials the cited reference on the form and that it be made
of record in the application and that a copy of the initialed
30 form be sent to Applicants with the next communication from
the Examiner.

Since the information disclosure statement is filed before the mailing date of a first Office action, the requirement set forth in §1.97(b) is satisfied. The Taiwan patent No. 444993 contained in the information disclosure statement was cited
5 in communications from the Taiwan Intellectual Property Office on 06/16/2004. Applicants sincerely hope that the examiner can consider the items contained in the information disclosure statement.

10 According to the requirement set forth in 37C.F.R. §1.98 and M.P.E.P. 609, the applicants are submitting a copy of the cited reference (TW No. 444993) and a concise explanation of the relevance is described hereinafter.

15 The cited reference provides an OLED driving circuit for decreasing a difference between a plurality of driving currents I_{out1} , I_{out2} by coupling the driving currents I_{out1} , I_{out2} in series, wherein each of the driving currents I_{out1} , I_{out2} is used for driving a pixel and is generated by a driving
20 integrated circuit (IC) 40, 50. Owing to the variation of the semiconductor process, the parameters of those driving ICs 40, 50 manufactured by the same semiconductor process are different accordingly. A first op-amplifier 42 is used for receiving an input voltage signal V_{BT} via a first input terminal.
25 Input terminals of a plurality of output transistors 441-44N are connected to an output terminal of the first op-amplifier 42, and output terminals of the output transistors 441-44N are connected to a second input terminal of the first op-amplifier 42 to form a close loop. In addition, the output
30 terminals of the output transistors 441-44N are further connected to the driving IC 50 for equalizing the driving currents generated from the driving ICs 40, 50. The cited OLED

driving circuit teaches that a first current mirror is connected to a first output transistor 441 for providing a plurality of currents I_1-I_n to the corresponding output transistors 441-44N. In addition, a resistor R is connected to the output terminal of the first op-amplifier 42 for adjusting the driving current I_{out1} .

In summary, the cited OLED driving circuit equalizes the driving currents generated from different driving ICs, which are used for driving the pixels to have the same gray level, by connecting the current mirror 46 of the driving IC 40 to another driving IC 50. Therefore, the driving current I_{out1} is equal to a current I_x flowing in the driving IC 50, and the current I_x is equal to the driving current I_{out2} generated from the driving IC 50 according to the characteristic of the current mirror 56 within the driving IC 50. As a result, the cited OLED driving circuit matches the driving currents of the driving ICs by connecting the driving currents in series.

20

Independent Claim 1 of the present invention is repeated here for reference.

1. A display controller for driving a monitor comprising:

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a graphics chip for outputting a display data; and a converter for converting the display data into a display driving voltage, the converter comprising:

30

a current mirror circuit for generating an output current according to a reference current and the display data, the output

current and the reference current
corresponding to a mirror ratio, the output
current being delivered to the monitor for
generating the display driving voltage; and
5 a voltage calibration circuit for modifying the
mirror ratio according to the display
driving voltage and a predetermined display
driving voltage and adjusting the output
current to drive the display driving voltage
10 to approach the predetermined display
driving voltage.

Compared with the cited OLED driving circuit, the display
controller 66 shown in Fig.3 comprises a current mirror circuit
15 82, 83a, 83b, 83c, and a voltage calibration circuit 68. The
kernel feature of the present invention is using a voltage
calibration circuit to modify the mirror ratio according to
the display driving voltage and a predetermined display
driving voltage for adjusting the output current. Then the
20 adjusted output current is capable of making the display
driving voltage approach the predetermined display driving
voltage. Therefore, when the display controller of the present
invention is used to drive different monitors having different
input resistances, the display controller is capable of
25 generating identical display driving voltages for driving
these monitors to show images corresponding to the same display
data. The same image, therefore, is successfully shown on
different monitors, and the display quality is greatly
improved owing to the voltage calibration circuit.

30

As mentioned above, the problem solved by the cited reference
is different from the problem solved by the present invention.

In addition, the cited reference fails to teach that a voltage calibration circuit is implemented in the driving circuit for modifying the mirror ratio of a current mirror to adjust the output current. It is thus believed that the cited reference
5 fails to teach all of the limitations in claim 1 of the present invention.

Independent Claim 11 of the present invention is repeated here for reference.

10

11. A method for calibrating a display driving voltage comprising:

15

(a) converting a display data into an output current according to a reference current, the output current and the reference current corresponding to a mirror ratio, the output current being used for generating the display driving voltage; and

20

(b) **comparing the display driving voltage and a predetermined display driving voltage for modifying the mirror ratio and adjusting the output current to drive the display driving voltage to approach the predetermined display driving voltage.**

25

As mentioned above, it is clear that the cited reference fails to teach the step of modifying the mirror ratio of a current mirror to adjust the output current. It is thus believed that the cited reference fails to teach all of the limitations in claim 11 of the present invention.

30

Respectfully Submitted,

5 Winston Hsu Date: 9/15/2004

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